

1 1. A memory comprising:
2 a first and a second layer of memory material
3 spaced from one another in a first direction; and
4 a first and a second address line extending
5 substantially in said first direction through said first
6 and second layers.

1 2. The memory of claim 1 wherein said memory
2 material includes a ferroelectric polymer material.

1 3. The memory of claim 1 including third and fourth
2 address lines which extend in a second direction different
3 from said first direction.

1 4. The memory of claim 3 wherein said first and
2 second directions are substantially transverse to one
3 another.

1 5. The memory of claim 3 wherein said third and
2 fourth address lines are in said first layer.

1 6. The memory of claim 5 including a first cell
2 formed in said first layer between said first and third
3 address lines and a second cell formed in said first layer
4 between said second and fourth address lines.

1 7. The memory of claim 6 wherein a bicell of two
2 cells is formed in said first layer on opposed sides of
3 said third address line.

1 8. The memory of claim 7 wherein said bicell is
2 formed between said first and second address lines, and
3 wherein said bicell includes said third address line.

1 9. The memory of claim 1 having more than two lines.

1 10. The memory of claim 1 having more than two
2 layers.

1 11. The memory of claim 1 wherein said layers are
2 vertically stacked.

1 12. The memory of claim 11 wherein successive layers
2 are spaced by an insulator.

1 13. The memory of claim 1 wherein said lines are vias
2 extending vertically, said memory including a substrate
3 having a surface, said first direction being substantially
4 transverse to said surface.

1 14. A method comprising:
2 forming a first and a second layer of memory
3 material, said first and second layers spaced in a first
4 direction; and

5 forming a first and a second address line
6 extending substantially in said first direction through
7 said first and second layers.

1 15. The method of claim 14 including forming a third
2 and fourth address line extending substantially
3 transversely to said first direction.

1 16. The method of claim 15 including forming said
2 third and fourth address lines in said first layer.

1 17. The method of claim 14 including forming a bicell
2 structure.

1 18. The method of claim 14 wherein forming a first
2 and second layer of memory material includes forming
3 ferroelectric polymer memory material layers.

1 19. The method of claim 14 including forming more
2 than two lines and more than two layers.

1 20. The method of claim 14 including forming said
2 lines by forming metal filled vias.

1 21. The method of claim 14 including forming an
2 insulator between said first and second layers.

1 22. A method comprising:
2 addressing a polymer memory using first lines
3 extending substantially in a first direction to address
4 cells defined in at least two layers spaced from one
5 another in said first direction.

1 23. The method of claim 22 including using second
2 lines extending substantially transversely to said first
3 direction to address cells between said first and second
4 lines.

1 24. The method of claim 23 including addressing a
2 bicell between a second line and two adjacent first lines.

1 25. The method of claim 23 including addressing a
2 cell in one layer by applying a potential to adjacent first
3 and second lines.

1 26. The method of claim 22 wherein addressing
2 includes addressing a ferroelectric polymer memory.

1 27. A system comprising:
2 a controller;
3 a wireless interface coupled to said controller;
4 and
5 a polymer memory coupled to said controller, said
6 memory including a substrate having an upper surface, a
7 plurality of first address lines extending in a first
8 direction, at least two layers of memory material spaced
9 from one another in said first direction, said lines
10 extending through said first and said second layers.

1 28. The system of claim 27 including a third and
2 fourth address line extending substantially transversely to
3 the first direction.

1 29. The system of claim 28 wherein said lines form a
2 bicell structure.

1 30. The system of claim 29 wherein said interface
2 includes a dipole antenna.

1 31. The system of claim 27 having more than two
2 lines.

1 32. The system of claim 27 wherein said polymer
2 memory is a ferroelectric polymer memory.

1 33. The memory of claim 27 having more than two
2 layers.

1 34. The memory of claim 27 wherein said layers are
2 vertically stacked.

1 35. The memory of claim 34 wherein successive layers
2 are spaced by an insulating layer.

1 36. The memory of claim 27 wherein said lines are
2 vias extending vertically, said substrate having a top
3 surface, said first direction being substantially
4 transverse to said surface.